eurocomp
The newsletter of the Space Components Steering Board

Introduction

Welcome to the fifth issue of Eurocomp, the newsletter of the Space Component Steering Board (SCSB). This issue is dedicated to the current developments underway to strengthen the European capability in integrated circuits for space missions.

Space missions, whether they are in the science or applications domain, engender major design challenges. Each mission has unique requirements for basic functionalities such as spacecraft control, data storage and management systems where integrated circuits play a major role. Along with the usual mass savings, cost, and performance (power/speed) improvements necessary, the radiation environment and its effects on electronic systems impose a supplemental demand.

In order to highlight the evolution of some of the enabling technologies that anticipate these demands, the Silicon Dossier, one of four technology dossiers that compose the five-year strategic plan, is presented. The four main themes behind this important initiative detail the efforts to maximise the existing resources and capabilities to provide the necessary components in the short and medium term.

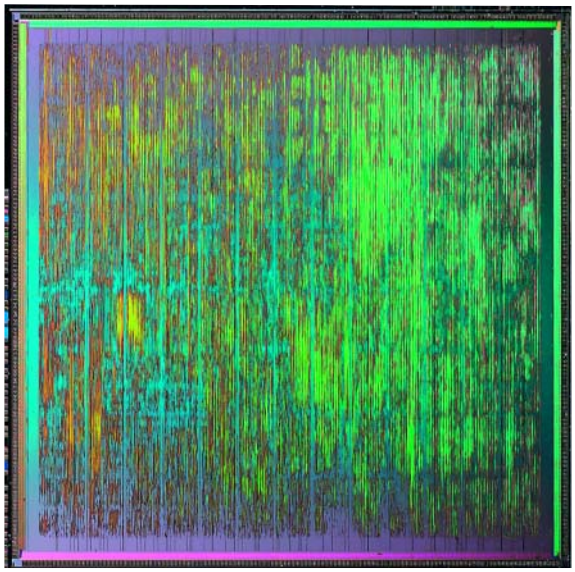
In this issue...

Present-day design trends emphasise the need for cost-effectiveness through coordinated and reliable design practices. In this light, a new ECSS standard for the development of Application Specific Integrated Circuits (ASICs) is being prepared. Similarly, a working group composed of experts from both agency and industry is working towards an ECSS design and development standard for Monolithic Microwave Integrated Circuits (MMICs).

While this issue concentrates on integrated circuits, we also draw attention to ‘ESCCON 2002’. September in Toulouse France is where the SCSB will showcase all of the developments in space components through this major conference. We do hope you will put attendance of this event in your calendar for 2002!

The 5-Year CTB Strategic Plan
- The Silicon Integrated Circuits Dossier

The past five years have been the most turbulent period so far in the history of the semiconductor industry, alternating rapidly between up- and downturns. Continuing the trend of consolidation, the industry is restructuring but so far without slowing the pace of innovation. Contrary to the major market segments, manufacturers still active in the military and aerospace sectors have enjoyed a more stable business climate. Various manufacturers have even reported growing revenues for these areas and have started to appreciate again the more steady evolution and profitability of this special market segment.



Die of Alcatel Space Industries DRAF ASIC, implemented on a 2.4 Msites Atmel 0.35 micron Rad Hard Sea of Gates, for the MT-SAT2 project

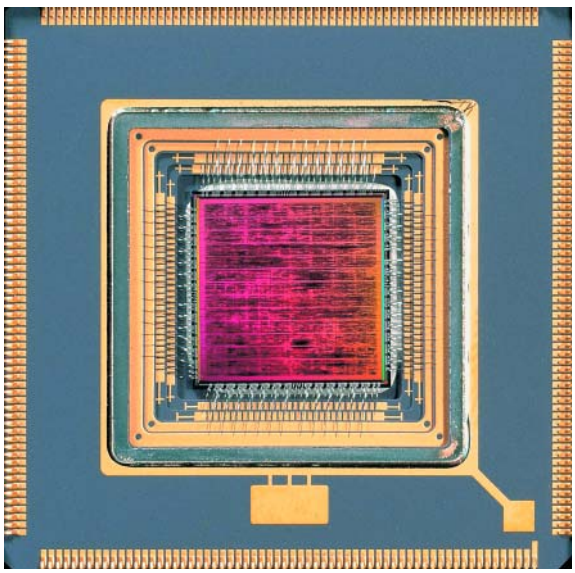
However, in absolute terms the volume of silicon produced for high-reliability applications still represents only a niche market, with less than 1% of the total. For the space industry, it will continue to be a challenge to benefit from the general progress in semiconductor technology. This means at least narrowing the gap between the current range of qualified or approved space components and state-of-the-art industrial capabilities.

To ensure the provision and ready availability of advanced high-performance Silicon Integrated Circuits in the broadest sense is the objective and the purpose of the Silicon Dossier. This is one of the four Dossiers compiled in 1998, and issued in 1999, that describes the strategic short- and medium-term needs of the European Space Industry in the area of EEE components. Although the Silicon Dossier is presently being revised, a task now undertaken by a newly formed specialist Working Group, its perspective and general recommendations are still valid and the resulting actions are progressing or being prepared for implementation.

Scope and structure

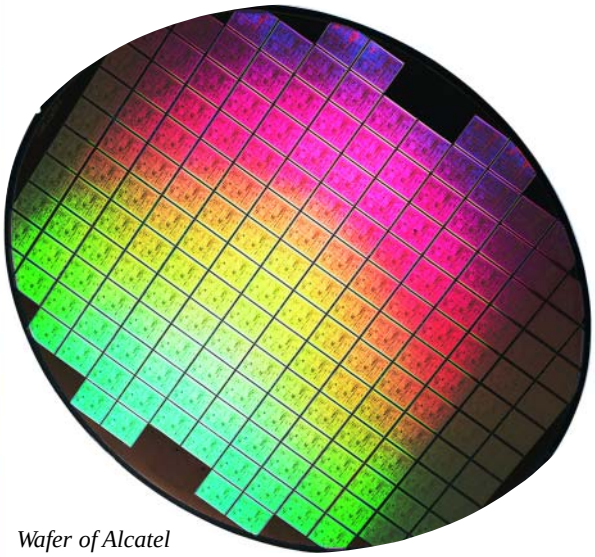
The Silicon Dossier is intended to cover all silicon-based components regardless of their function, complexity or process technology, unless they are covered by other more specialised Dossiers like the Photonics Dossier. However, in line with the primary intention to first of all define strategic needs, the first issue of this Dossier has been restricted to the most critical technologies and component types. For example, it does not yet include discrete or power devices. The focus is placed on Integrated Circuits (ICs) for digital, analogue and mixed signal applications, with some attention paid to the emerging and maturing area of Micro Electromechanical Systems.

The Dossier provides background information, the declaration of needs, analysis and recommendations. The background information includes the current status of silicon technology and products, European manufacturer capabilities compared to their



Packaged die of Alcatel Space Industries DRAF ASIC, implemented on a 2.4 Msites Atmel 0.35 micron Rad Hard Sea of Gates, for the MT-SAT2 project

competitors, and a brief reflection on technology and semiconductor market trends. The compilation of needs is based primarily on Eurospace, ESA, CNES and other space-agency inputs provided to the Component Technology Board (CTB), which includes confirmed as well as anticipated component requirements. The recommendations are grouped into four main themes reflecting the strategic lines to be followed. Within each of these themes, a series of more or less specific recommendations are made.



Wafer of Alcatel Space Industries DRAF ASIC implemented on a 2.4 Msites Atmel 0.35 micron Rad Hard Sea of Gates, for the MT-SAT2 project

It is important to note that the Dossier is not a work plan, but defines a set of objectives. Recommendations may result in multiple parallel activities, or a series of sequential activities. Their effective implementation is subject to technology/industrial readiness and budget availability. It is therefore a further and separate task of the CTB to coordinate the implementation of activities within the Annual Qualification Plan or as part of the appropriate technology programmes of the SCSB partners.

Theme 1: Ensuring Radiation-Hard Technology from European Sources

European Space Projects have always depended on non-European sources for the supply of many radiation-tolerant or radiation-hard component types. As this dependence has gradually increased over the past years, it is considered to be a strategic necessity to reverse this trend. A substantial European capability for the design and production of radiation-tolerant and radiation-hard space components therefore needs to be created and maintained.

- Accordingly, it was recommended to pursue the qualification of the Atmel 0.35 micron CMOS process and Sea-of-Gates technology, which have been radiation-hardened with the help of CNES and ESA funding, and to continue with a similar radiation hardening, evaluation and qualification programme for the next generation 0.25 micron CMOS process and standard-cell technology.
- Further recommendations refer to the qualification of several standard component types developed previously in other radiation-hard or -tolerant Atmel processes, such as the TSC21020 Digital Signal Processor and its companion devices currently under development or the single-chip SPARC microprocessor.
- Another recommendation calls for the development of an alternative radiation-hard process emerging from European research institutions.

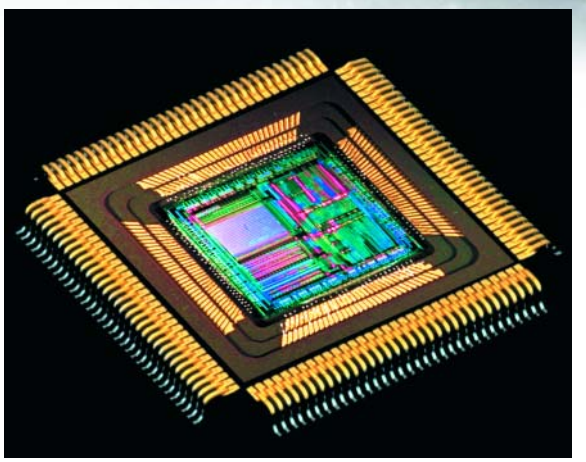
Theme 2: Use of Other Existing European Foundry/Component Capabilities for Space

In order to further strengthen the remaining European space-component suppliers and to broaden the number of sources in the future, the following actions were proposed:

- Implementation of a multi-year design initiative to exploit commercially available technologies by radiation hardening of existing components, by design when appropriate or migration to more radiation tolerant processes, e.g. linear components, low-voltage standard logic, non-volatile memories.
- Evaluation of an advanced low-power CMOS technology with Cu interconnect and embedded volatile/non-volatile memory capabilities from a European source.
- Evaluation of an advanced BiCMOS technology for analogue and mixed analogue/digital applications.

Theme 3: Provision of Advanced Commercially Based Components

The development of innovative high-performance electronic systems for space applications will also require the use of technologies and component types that are not, and may not become available from space-qualified manufacturers. It is therefore deemed necessary to implement a systematic, phased evaluation programme covering a broad range of advanced industrially available device types. As a matter of efficiency, this should be based on a continuous survey of emerging products to identify and select part types for an initial radiation characterisation followed by a tailored reliability evaluation for parts meeting minimum radiation tolerance levels. In particular, this set of recommendations calls for, for example:



Atmel packaged Rad Hard 21020 DSP

- The evaluation of high-complexity FPGA/CPLD component families employing one-time and reprogrammable technologies. A radiation pre-screening programme that had already been initiated by ESA will be continued in response to this item.
- The initiation of pre-evaluation activities for the selection of lower end, 8/16-bit micro-controllers/micro-processors and future high-performance CISC/RISC and DSP processors.
- A periodic radiation pre-screening programme for short life-cycle components, such as volatile and non-volatile memory components, providing for at least one multi-type test campaign per year.
- The evaluation and qualification of high-speed-bus interface components in particular for systems configured around the SPARC microprocessor and the TSC21020 DSP. This includes component types under development for the Spacewire IEEE 1355 based serial link.
- The evaluation and qualification of suitable existing linear ICs such as MOSFET drivers, operational amplifiers, comparators and regulators to replace obsolete or less efficient part types. Optionally, the activity should include the redesign or development of selected functions with a European foundry, if necessary. The focus will be on the component types needed for on-board power systems.
- The evaluation and qualification of suitable high-speed 8- to 9-bit ADCs supporting 1 GHz sampling rate or higher (which might require GaAs/SiGe technologies addressed under the Microwave Programme) and 10 bit with 60 MHz or more.
- The definition and implementation of an Obsolescence Management System as a systematic and effective tool to deal with the decreasing process and product life cycles, as well as the consequences of continued restructuring of the semiconductor industry. Such a system will require a cooperative effort between the user industry, space component manufacturers, procurement agents and space agencies. This includes the monitoring of procurement activity and industrial changes to plan and initiate the timely replacement of critical components.
- Further studies directed towards the identification of alternative, innovative approaches, e.g. for technology and components, radiation-hardening by electrical and shielding design, and radiation testing.

Theme 4: Special Actions

To support the strategic actions it is recognised that the existing approach to requirements will need to change and new concepts and methods will need to be introduced. Accordingly an additional set of special actions have been defined:

- Establishing minimum testability and test-coverage standards for space ASICs.
- The definition and promotion of a system for the exchange of Intellectual Property (IP) cores for the space-application domain, preferably as an extension of emerging industrial approaches. This approach should also be extended into a practical concept for Application-Specific Standard Products (ASSPs).
- The development and demonstration of evaluation and qualification methods for MEMS, in combination with advanced application developments like the solid-state gyroscope development.

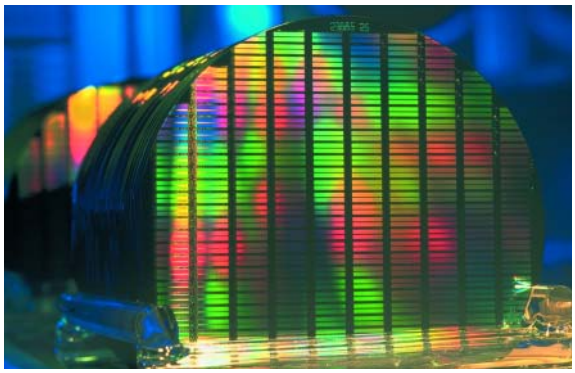
Progress achieved

A considerable number of the recommendations proposed serve to complete initiatives taken in the past or which are currently in progress and are aimed at securing investments, as well as assuring a practical level of continuity. Other recommendations are meant to prepare for a broader European supply base, but require the continuous updating of IC needs, in terms of functionality, performance and scope of application by space-system manufacturers. This will facilitate a focused search of available European technologies and suppliers for suitable sources.

In 2000, a three-year programme aimed at developing next-generation ICs for space applications was agreed between ESA, CNES and ATMEL Nantes (subsidiary of ATMEL Corporation). This programme covers the following main activities:

- Radiation hardening of the AT56K 0.35 micron CMOS process (completed) and the related

evaluation programme (to be completed in 2002).
- Development of a radiation-hardened library for the AT56K 0.35 micron CMOS rad-hard process and the related evaluation of the 0.35 micron ASIC offering according to the ESA/SCC System (completed).
- Radiation hardening of the AT57K 0.25 micron CMOS process (on-going) and the related evaluation programme.



Atmel batch of wafers in a carrier at the end of the Si process

- Development of a radiation-hardened library for the AT57K 0.25 micron CMOS rad-hard process (started in Q4 2001) and the related evaluation of the 0.25 micron ASIC offering according to the ESA/SCC System.
- Development of SEU-free FPGA, based on the 0.35 micron CMOS RT process (started in the second quarter of 2001 and to be completed in 2003).
- Evaluation of SPARC™ SC (TSC695) according to the ESA/SCC System (completed end-2001).
- Development, radiation characterisation and evaluation of the SPARC™ New Generation (NG) processor based on the LEON micro-processor designed at ESA (on going).
- Development and evaluation according to the ESA/SCC System of a 4 Mbit SRAM for space applications (on-going and to be completed in 2003).
- Development of flip-chip and new space-assembly technologies to meet the needs for high-density packages (to be completed in 2003).

A continuing radiation pre-evaluation programme has been addressing a wide range of FPGA, memory and data-handling device types. Many of the results have already been reported and are available for downloading from the ESA Radiation Database located in the public area of ESCIES. The most recent results were presented during the annual QCA Final Presentation Day at ESTEC in Noordwijk (NL) on 9 April 2002 and will soon be included in the database. A large number of specific activities responding to the recommendations made in the Dossier are in an advanced preparation stage and will be initiated under ESA and CNES contracts in the near future.

Updating

In order to support a frequent updating of the Silicon Dossier, and as now in place for all Dossiers, a permanent expert Working Group has recently been created by the CTB. Its first meeting is foreseen for early in 2002, with a view to completing the first revision, which is already in preparation, by April 2002.

MMIC Technology within the ECSS and ESCC Standards

The establishment of standards/specifications for III-V Monolithic Microwave Integrated Circuits (MMICs) for space applications in accordance with the ESCC System and ECSS-Q-60 has been assigned to an Implementation Team (IT) sponsored expert working group. The latter reports to and receives directives from the IT chairman (F. Linder, CNES). The group involves several specialists in the field from European semiconductor manufacturers (OMMIC and UMS), space companies (Alcatel Space Industries, Alenia, Astrium, Bosch Satcom) and agencies (CNES, ESA).

According to the Cooperation Agreement between the ESCC and the ECSS, it is the intention to develop space-project standards relating to general procurement, including the design and selection of EEE components. The MMIC Working Group will strive to define the ‘best space practice’ to develop, design, qualify and procure RF dice to be used in hybrid equipment for space application. The methodology will be the basis of a new common approach to be defined by the manufacturers, the industries and the agencies.

It is intended that requirements related to product manufacturing, evaluation, qualification,

performance, QML approach, and capability approval be developed under the ESCC system, which is a system of EEE component specifications developed for qualification and procurement uniquely for space applications.

The MMIC Working Group will draft ESCC and ECSS documents to be issued in May 2002 as follows:

- A Level-3 standard under the ECSS-Q-60 series. The task will be to introduce a draft document that will incorporate requirements for the design, selection, procurement and use of MMICs.
- Introduction of requirements addressing die issues through the updating of ESCC 9010 for MMIC procurement including structural and/or technical changes (the CNES guideline MPM 52-10-10 will be used as an input to implement the Level-3 ECSS-Q-60 and the ESCC 9010 documents).
- An update of ESCC Basic specification 2549010 for MMIC QML approach (the requirements of SCC Basic Specification 25400 will be taken into account, and amended if necessary). The requirements may be adapted for chip form qualification.

The ESCC QML will entail basic rules and requirements for evaluation and qualification leading to a QML programme, as well as requirements, test methods, accept/reject criteria for qualification, production, and procurement of MMICs for space applications.

The ECSS Level-3 standard will define either guidelines or requirements for the design, selection, procurement, and use of MMICs.

Furthermore, consultation with worldwide industrial partners (including other European and major US semiconductor companies) will form part of the activities and will allow the concept and methodology to be validated. This will be a key element in the successful definition of these standards.

Readers may request additional information, or make proposals regarding the on-going activities, by contacting the author :

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Preparation of ECSS Standard for ASIC Development – ECSS Q-60-02

Scope

In order to achieve compact lightweight electronics with high functionality, Application Specific Integrated Circuits (ASIC) are widely used for space projects. In the past, the design, development, and testing of ASICs were carried out either according to the in-house procedures of the design companies, or to a set of requirements agreed between the user and the designers.

The user community recognised a need to develop a harmonised European standard that addresses the ASIC development process specific to space applications. Furthermore, the standard shall be issued in the European Cooperation for Space Standardization (ECSS) system.

The new Standard is intended to serve as a tool and will improve visibility during the development process to avoid unnecessary iterations. In addition, it will serve as a basis for discussion between designers and parts experts to take into account appropriate measures for requirements such as the necessary radiation-hardening schemes and the testability concepts. The aim is to ensure that the final design will operate reliably for space missions.

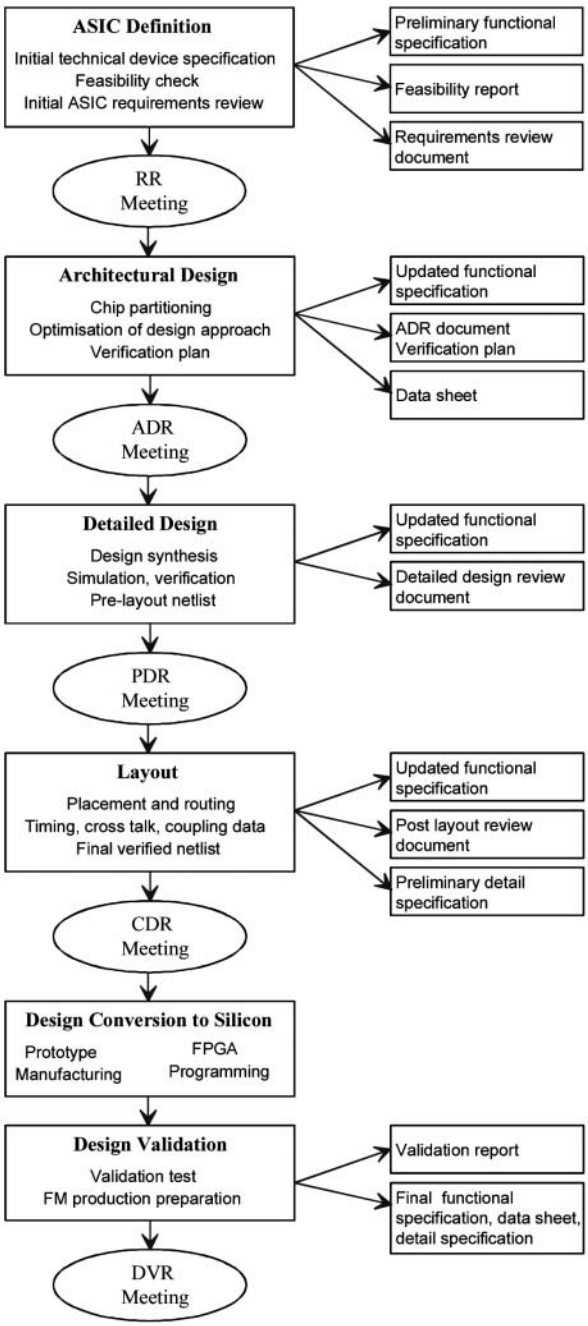
The proposed Standard will also consolidate and update ASIC design and assurance requirements as presently defined in various ESA and industry documents. As a unified requirements document, it will be applicable to the broad scope of full- and semi-custom-designed ASICs (excluding MMICs), implementing digital, analogue or mixed signal functions based on the available range of technologies, design approaches and tools. It will also be applicable to some extent to the use of programmable logic devices and FPGAs.

Approach

The preparatory work for the new Standard began with a review of design flows for state-of-the-art processes suitable for space application. By comparing these various design flows, three general

flows dedicated to digital, analogue and FPGA design, containing general applicable design steps, were derived. An overall development flow was then established and assessed during discussions with ESA experts.

The development flow generated (see below) spans the entire implementation, from initial requirements and technical device specification, up to and including design validation and the necessary preparations for production of the flight models.



The layout of the new document follows the current rules for ECSS documents, with sections such as Foreword, Introduction, and Scope and a chapter division consisting of management, engineering, and quality assurance.

Subsequently, the existing ESA documents were reviewed and the relevant requirements from these documents were incorporated into individual chapters of the new Standard. As the existing documents are essentially related to digital design, additional requirements for analogue design and for FPGAs were added.

Industrial review

The second issue of the draft Standard was distributed to a European expert group (semiconductor vendors, design houses, users, National Space Agencies and institutions) for comment. This input will ensure that their specific requirements are adequately taken into account. In total, 55 contact persons all over Europe were included in this consultation.

In addition, an Internet site has been established (within ESCIES) to aid in the review process. This tool allows participants to download the draft Standard and to input comments directly referring to specific chapters. These comments, in turn, are accessible by the whole community of contact persons, enabling continuous direct exchange within this group of experts.

TeSat* visited two ASIC vendors to discuss the draft Standard in more detail. Many companies also conducted internal co-ordination meetings to harmonise their comments.

The majority of the comments collected approved of the chosen approach and confirmed the applied layout in general. They helped to focus existing requirements and to complete those for analogue, mixed-signal and FPGA design. In particular, the integration of the specific stages of FPGA design into the overall flow has been promoted.

All of these improvements have been introduced in the third issue of the draft ECSS Standard, which has been distributed to European Industry together with an invitation to an industrial review meeting to be held at ESA at the beginning of 2002. It is intended that this consolidated industrial review should resolve all outstanding issues and result in a final draft of the ECSS Standard. This draft version will then be converted into an approved ECSS Standard, with a target release date of May 2002.

* TeSat (D) is preparing the Standard under ESA contract.

ESCCON 2002:
European Space Components Conference

The ESCCON will be held in September 2002 in Toulouse, France. It is the only European Conference specifically dedicated to Space Components. The SCSB sponsor this biennial forum for managers, engineers and scientists working in the field of components and technologies used in space programmes - satellites, launchers and manned space missions.

The rapid evolution of mission requirements is a permanent challenge for component engineers. New management concepts, qualification methodologies and improved procurement approaches for high-reliability and commercial components are some of the answers to these challenges, and these will be addressed at the Conference. Results from within the framework of the ESCC initiative will be particularly highlighted.

In addition, the 'state of the art' and the main technology trends for components, packaging and assembly and their suitability for space use, will be an important part of the Conference, as well as the associated developments in evaluation, qualification and reliability prediction procedures. Activities dealing with the selection, procurement and use of components for space applications will also be emphasised.

ESCCON 2002 will build on the success of the previous Conference to promote a broad exchange of views between participants from various projects and countries from around the world.

Papers will be distributed between three main themes proposed by the SCSB. The first theme will deal with activities performed as part of the European initiative (ESCC). The second will cover component and technology engineering, and the third component quality assurance and procurement.

For more details please visit:
https://escies.org/public/esccon2002.html

Published by: ESA Publications Division
c/o ESTEC, PO Box 299, 2200 AG Noordwijk, The Netherlands
Tel. (31) 71 565 3400 - Fax (31) 71 565 5433

Editor: Bruce Battrick

Layout: Eva Ekstrand

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