Radiation-Hardness Components at Scaled Technology Nodes (UTBB FDSOI28) – Test of Single-Events Effects in ARM Cores

Study Reference Number: 15-7002
Type of activity: Standard study (30 k€)

Project Summary

Objective

This project will investigate radiation-hardness aspects at scaled semiconductor technology nodes, below 65nm, targeting specially to test UTBB FDSOI 28 nm technology.

Target university partner competences

Circuit design, radiation test vehicle design, circuit simulation, radiation simulation codes

ACT provided competences

Nanotechnology, radiation-matter interaction physics

Keywords

UTBB FDSOI 28 nm, RHBD, ARM, Single-Event Effects, Single-Event Transient

Study Objective

This study aims to investigate radiation-hardness aspects such as Single-Event Effects (SEE) for electronic components at scaled technology nodes using UTBB FDSOI 28nm. In particular, system test of this technology for ARM processor cores with several strategies of radiation-hardness by design is aimed at. Results and design strategies would be important deliverables of the project regarding an assessment of this technology for reliable electronic components for space applications.

Background and Study Motivation

The space radiation environment is a key challenge for all types of space missions particularly because it can affect the operation of spacecraft electronics leading to performance degradation or even catastrophic failure. The resulting effects of this interaction are commonly referred as total ionizing dose (TID), displacement damage (DD) and single-event effects (SEEs). TID is the cumulative damage caused by ionizing radiation over the time of exposure, inducing transient photocurrents and in the long-term creating leakage paths and threshold shifts. SEE results from a high-energy particle traveling through a semiconductor and leaving an ionized track behind, which can cause bit-flip, latch-up or burnout. To cope with these aspects, the space industry can rely on commercial off the shelf components (COTS), Radiation Hard by Process components (RHBP) or

Radiation Hard by Design components (RHBD). The unsuitability of COTS and the effort and cost of a RHBP component makes RHBD components the standard solution. RHBD strategies include triple mode redundancy (TMR) within layout, dopant well and isolation trenches circuit layout design, error correction circuitry (ECC) and device spacing and decoupling design rules.

In later years the total dose hardness (TID) of commercial solutions has improved mainly due to technological improvements in thin gate oxides and increasing semiconductor doping levels. However with current scaling in COTS technology, SEE are indeed a reliability concern for sub-65 nm CMOS due to the small amounts of charge representing each bit (fC range), high clock speeds, low operating voltages and high packing densities [1]. On the other hand, the semiconductor industry has developed new technological solutions to continue scaling below 45 nm, such as FinFETs multi-gate transistors and Ultra-Thin Body & BOX Fully Depleted Silicon On Insulator (UTBB FDSOI). STMicroelectronics started production of FDSOI at 28 nm node in 2013, aiming to increase circuit performance and reduce circuit power consumption until the 10 nm node [2, 3]. Despite the reliability concerns mentioned above, in FDSOI the combination of SOI with high doping levels in the body region results in insensitivity to TID [4]. Also, as analysed in [5] the reduction of the sensitive volume for this technology resulted in increased robustness to SEE. This explained the lowest failure-in-time (FIT) rate ever observed (<10 FIT/Mb for high-energy neutrons) for COTS SRAMs [5] when compared against FinFET, bulk and other technologies.

Further, the indication of intrinsic hardness against radiation of this technology was not only confirmed in SRAMs [5, 6, 7, 8] but also in SPARC-V8 microprocessors tested against alphas and neutrons [9, 10].

Based on the previous reported results, the radiation hardness of this technology could be used as the brick for new rad-hard microprocessors in space applications. In particular, considerable attention is being given to ARM architecture microprocessors as low-power, low-cost alternatives for general-purpose computing. This is supported by the recent developments of space rad-hard cores ARM Cortex-R4 by ARM [11] and ARM Cortex-M0 by SST [12] at 130 nm node.

Therefore, an ARM microprocessor in UTBB FDSOI 28 nm would be an interesting research candidate, not only because of the preliminary results referred above but also regarding questions of suitable RHBD techniques at these nodes.

Being complex circuitry, microprocessors are sensible to all sorts of SEE such as single-event upset (SEU), single-event transient (SET), single-event functional interrupts (SEFI) or single-event latch-up (SEL) which can result in a multitude of microprocessor's failure modes. To perform testing in an efficient and repeatable manner requires *accelerated testing* where devices are exposed to various high-intensity radiation sources that reproduce the space radiation environment. The tests should be performed in an automated test vehicle in agreement with JEDEC JESD89A (memory and logic components) and ESA/SCC basic specification number 25100 (for SEEs). This test vehicle should remotely control (through a tester hardware board) a small number of devices under test (DUT board) at a time while being irradiated. The testing parameters are power supply voltage, device's access method and speed and test pattern. The vehicle operating mode can be static or dynamic. When dynamic, the DUT is initialized before irradiation to a known state, once irradiation starts the DUT is accessed continuously, at a specific rate in the test plan, and error events are counted while they are detected. Dynamic testing combined with real-time current consumption monitoring at component level, allows discrimination between different error types including single-bit upset (SBU), multiple-bit upset (MBU), single-event functional interrupt (SEFI), SEL or even SET in some vehicles [13].

This also highlights the importance of the testing control software, which can be as specific as in [14, 15] identifying with high precision the different failure modes of a given processor while performing a certain computation.

In summary, in this study, the radiation testing of an ARM architecture with several types of RHBD in UTBB FDSOI 28 nm for SEE (using the described accelerated testing) is intended. The results of the study could lead to a comprehensive assessment of this technology and pave the way for their introduction in space applications.

Proposed Methodology

The following study logic is proposed, though proposals of different approaches to achieve the main goals of the study are also welcome:

- Confirmation of suitability with modifications of the test vehicle reported in [16] for ARM processor core test with different levels of RHBD such as TMR and DICE flip-flops.
- Test vehicle setup mounting and test plan implementation for accelerated testing (software control of hardware tester programming).
- Irradiation tests on ARM cores for SEE (with heavy ions, protons, neutrons, …) in suitable facility.
- Measurement of static and dynamic SEE cross-sections as function of LET with pre-defined test pattern. Results could show correspondence between microprocessor failure mode and single-event type if possible.
- Investigation of clock speed influence in radiation-induced microprocessor failure such as in [14, 15], if possible.
- Investigation of different RHBD techniques on results.

The tests are expected to agree with JEDEC JESD89A and ESA/SCC basic specification number 25100 standards.

ACT Contribution

This study is addressed to research groups having expertise in circuit design, radiation test vehicle design and radiation experimental test.

The project will be conducted in scientific collaboration with ESA researchers. In particular ESA researchers will provide expertise in space standards, space qualification testing and radiation-matter interaction. ESA researchers would be specially involved in design review and result analysis.

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