Fundamentals of Memristors

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The day MEMRISTOR became famous...

The missing memristor found
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$$M(q) = R_{OFF} \left( 1 - \frac{\mu_V R_{ON}}{D^2} q(t) \right)$$

• RRAM seen as practical realisation of a theoretically predicted element
• Triggered a lot of interest especially in the EE (circuit design) world
Outline

1. What are memristors?
2. Do real memristors exist?
3. Generalized memristive systems
4. Non-pinched hysteresis
5. Do we need memristors?
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Memristor = the missing 4th element
Memristor = the missing 4th element

Figure 1 | The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor. Resistors and memristors are subsets of a more general class of dynamical devices, memristive systems. Note that $R$, $C$, $L$ and $M$ can be functions of the independent variable in their defining equations, yielding nonlinear elements. For example, a charge-controlled memristor is defined by a single-valued function $M(q)$. 
Mathematical Description

- \( M(q) = \frac{d\phi}{dq} \)

\[
\frac{d\phi}{dt} = M(q) \frac{dq}{dt}
\]

\[
V = M(q) I
\]

\( \rightarrow \) \( M \) has dimension of resistance [Ohm]

\( \rightarrow \) \( M \) depending on integral of passes current : memory

\( \rightarrow \) name of MEM-RISTOR
Pinched hysteresis loop

\[ v = M(x).i \rightarrow i = 0 \rightarrow v = 0 : \text{zero crossing} \]

“if it’s pinched, it’s a memristor” (L. Chua)
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Prototypical device = (TiO2 based) RRAM
Device Model & Formula's

- Total $R = \text{series connection}$
  - $M(t) = R_{ON} \cdot W(t)/D + R_{OFF} \cdot (1-W(t)/D))$
  - $W(t) = \text{state variable}$
    - $\frac{dW(t)}{dt} = \mu \cdot E$ (drift of ions)
    - $E = R_{ON} \cdot i(t)/D$ (relation $E-i$)
    - $W = \text{function of the amount of charges passed through the device}$
  - $M(q) = R_0 - m \cdot R_{ON} \cdot \Delta R \cdot q(t)/D^2$
    - $R_0 = R_{ON} \cdot W_0/D + R_{OFF} \cdot (1-W_0/D)$
Physical?

Concept:
- Assumes special case of interfacial switching:
  - Current determined by layer resistivity, no influence by Schottky contact
  - Not proven, even not that it is interfacial and not filamentary (see further hysteresis loop)

- Need to account for generation/recombination of oxygen vacancies;
  - Possibly by REDOX reactions at interface

- We will have Oxygen Vacancy profiles (not 2 fixed levels, no abrupt transition...)
Physical?

- Movement of boundary is essentially FIELD driven, not CURRENT driven
- Further (for memory it needs to be) very non-linear: (good threshold behavior)
  \[ \frac{dW(t)}{dt} = \mu(E).E \]
- Link to current as through relation of electric current in the device with field: \( i \sim E \)
  - However, also in principle non-linear over whole operation range (including “switching”) (and different from drift non-linearity
- In memory we want at low fields (ideally) NO ion drift BUT measurable (state dependent) current, and “state change” only at high field:
  - Same integral of current at low field has different effect than integral of current at high field → not accounted for?
Hysteresis curve

▶ Theory:
- Each point on the pinched hysteresis is a stable point
- Limited change of dynamics over the complete range:
  ▪ as only linearly depending on the current level

▶ Real device:
- In different parts of the hysteresis, very different dynamics:
- Below Vt (SET) and V_{trans} (RESET) NO change of state
- 3 regions of state change:
  ▪ Snapback: very rapid initial set (impossible to control intermediate state)
  ▪ Second part of SET: state depending on CURRENT LEVEL (not charge) * microscopic still voltage controlled
  ▪ RESET: Voltage controlled
Hysteresis shape: memristor vs real

Model calculations

Real device

Memristive modeling - Three basic evaluation criteria

Essential characteristics of RRAM type cells

1. Non-symmetric I-V curve
2. Non-linearity of the switching kinetics
3. CRS in anti-serial connection of two devices
Memristive modeling - Three basic evaluation criteria

1. Non-symmetric I-V curve
2. Non-linearity of the switching kinetics
3. Anti-serial connection of two devices

Initial memristor model:

\[ \dot{x} = h(x, I) = K_1 \cdot I \cdot f(x, I) \]

\[ V = R(x) \cdot I = (\left( R_{\text{LRS}} - R_{\text{HRS}} \right) \cdot x + R_{\text{HRS}}) \cdot I \]

Joglekar's window function

\[ f(x) = 1 - (2x - 1)^{2p} \]
1. Non-symmetric I-V curve
2. Non-linearity of the switching kinetics
3. Anti-serial connection of two devices

1. Basic I-V curve

Symmetric I-V!

2. Non-linearity of the kinetics

Real device: exponential kinetics!

$t_{SET} \sim \frac{1}{V_p}$

Memristive modeling - Initial memristor model

1. Non-symmetric I-V curve
2. Non-linearity of the switching kinetics
3. Anti-serial connection of two devices

3. Anti-serial connection

No CRS behavior!

1. Linear I-V curve
2. Non-exponential switching kinetics
3. No CRS behavior

⇒ More realistic models are required

Other possible implementations?

Physical systems that do follow the resistance model (series connection or modified parallel connection):

\[ R_{c\prime} \alpha \quad R_{c} \]
\[ R_{N}(1-\alpha) \]

→ Systems with resistance based on polarization and position of domain walls:
  - Magnetic spin based devices (MTJ’s)
  - Ferroelectric Tunnel Junction
MTJ based Memristor?

– Standard STT-MRAM cell:
  • In principle:
    – resistance is depending on the angle between the magnetization direction in free and fixed layer
    – Angle can be changed by current
  • In practice: very fast dynamics:
    – For practical frequencies, no continuous hysteresis loop but abrupt jumps between 2 levels

\[
\frac{d\theta}{dt} = \alpha \gamma H_k (-\sin \theta \cos \theta + p \sin \theta)
\]
\[
p = \left(\eta \hbar I / 2\alpha e M_s H_k V\right)
\]
MTJ based Memristor?

- Devices based on domain wall motion in free layer
  - in plane current device or perpendicular current devices
- DW motion is current driven!!

\[
M(q) = \left[ R_H - \frac{(R_H - R_L)\Gamma q(t)}{D} \right]
\]

\[
\frac{dx}{dt} = \Gamma I.
\]

![Diagram of domain wall motion in free layer and pinned reference layer]
MTJ based Memristor?

Small changes!
In this case, going to extreme case annihilates DW


Idea: introduce a magnetic domain wall
→ multi-resistance state memory
→ sub-ns switching
FTJ based Memristor?

- Resistance depending on amount of up/down domains

Large resistance changes!

Figure 1 | Tuning resistance and ferroelectric domain configuration with voltage amplitude. a, Dependence of the junction resistance measured at \( V_{\text{sett}} = 100 \text{ mV} \) after the application of 20 ns voltage pulses \( (V_{\text{pulse}}) \) of different amplitudes. The different curves correspond to different consecutive measurements, with varying maximum (positive or negative) \( V_{\text{pulse}} \). b, Variation of a similar capacitor resistance with the relative fraction of down domains extracted from the PFM phase images. Red (and blue)-framed images show states achieved by the application of positive (and negative) voltage pulses of increasing amplitude starting from the ON (and OFF) state. The blue and red symbols correspond to the experimental resistance value as a function of the fraction of down domains extracted from the PFM phase images; the black curve is a simulation in a parallel resistance model. The error bars are calculated from the distribution of clear and dark contrasts in the grey level histograms. c, d, Current versus voltage curves, measured at 1 kHz on a similar capacitor, for various amplitudes of the maximum voltage (c) and current versus voltage curves, measured at different frequencies: 100 Hz and 10 kHz (d). e, Evolution of the inverse of the negative switching field as a function of the measurement frequency. The green circles are extracted from c, d, and the orange squares from \( R(V) \) curves similar to a at different pulse durations.
FTJ based Memristor?

- State variable $s = \text{fraction of down polarized domains}$
- Change of $s$ is field dependent

$$\frac{ds}{dt} = (1-s) \times \left\{ \frac{2}{\tau_p(V)} \left( \frac{t - \tau_N(V)}{\tau_p(V)} \right) \right\} = f(s, V, t)$$

- They claim if corresponds to the generalized conditions for memristor systems?

$$V(t) = R(\sigma, V, i) i(t)$$

$$\frac{d\sigma}{dt} = f(\sigma, V, t)$$

$$\dot{x} = f(x, v, t)$$

$$i = G(x, v, t) v$$

- OK if written in conductance...
FTJ based Memristor?

- Hysteresis curved shows different dynamics for SET and RESET?
  - Looks *suspiciously similar* to filamentary resistive switching???
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Real Resistive Switching Elements (RRAM)

- Do not comply with Memristor definition
- Can be viewed as Memristive Device
Memristor: special case of Memristive System

**Memristor\(^1\)**
(ideal memristor\(^2\))

Current controlled memristor:

\[ V = R(q) \cdot I \]
\[ \dot{q} = I \]

Voltage controlled memristor:

\[ I = G(\phi) \cdot V \]
\[ \dot{\phi} = V \]

\(q\): charge (integral of the current)
\(\phi\): magnetic flux (integral of the voltage)

**Memristive system**
(generalized memristor\(^2\))

Current controlled memristive system:

\[ V = R(\mathbf{x}, I) \cdot I \]
\[ \dot{\mathbf{x}} = f(\mathbf{x}, I) \]

Voltage controlled memristive system:

\[ I = G(\mathbf{x}, V) \cdot V \]
\[ \dot{\mathbf{x}} = f(\mathbf{x}, V) \]

\(\mathbf{x}\): inner state variables

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Even more general definition (time variant)

Dynamical system

\[ y = h(x, u, t) \]
\[ \dot{x} = f(x, u, t) \]

\( y \): output variable
\( u \): input variable
\( x \): internal state

Memristive system

\[ y = h(x, u, t) \cdot u \]
\[ \dot{x} = f(x, u, t) \]

\( y \): output variable
\( u \): input variable
\( x \): internal state

Scalar; current \( I \), voltage \( V \)

Multi-dimensional

Multidimensional
Current controlled memristive system:

\[ V = R(\mathbf{x}, I) \cdot I \]
\[ \dot{\mathbf{x}} = f(\mathbf{x}, I) \]

Voltage controlled memristive system:

\[ I = G(\mathbf{x}, V) \cdot V \]
\[ \dot{\mathbf{x}} = f(\mathbf{x}, V) \]

\( \mathbf{x} \): inner state variables

Property needed for pinched hysteresis loop:

\[ R(\mathbf{x}, 0) \neq \infty \]
\[ G(\mathbf{x}, 0) \neq 0 \]

Nonvolatile property:

\[ f(\mathbf{x}, 0) = 0 \]

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Hysteresis in actual RRAM system does NOT go through the origin!
EXTENDED Memristive devices

Figure 5 | Classification of mem devices. (a) Memristive, memcapacitive and meminductive devices are assumed to offer pinched characteristics at the origin in general\textsuperscript{39}. In the case of memcapacitive and meminductive devices, a spontaneous polarization of a ferroelectric and ferromagnetic material, respectively, leads for example, to non-zero-crossing characteristics\textsuperscript{11}. Similarly, a non-zero-crossing $I$-$V$ characteristic of a memristive device indicates the presence of an inherent nanobattery, that is, this device is active. Therefore, we introduce the generic terms extended memristive device, extended memcapacitive device and extended meminductive device to account for both zero-crossing and non-zero-crossing $I$-$V$ characteristics. Note that the origin of non-zero-crossing behaviour in memcapacitive and meminductive devices is of completely different nature than in memristive devices, thus require specific modifications of the concept. Interestingly, spin-transfer torque (STT) MRAM cells offer zero-crossing in contrast to ReRAM cells, thus can be considered as conventional memristive device. (b) Equivalent circuit of the extended memristive element. The ionic current is defined by the nanobattery, which controls the state-dependent resistor representing the electronic current path. The capacitance of the device is neglected as its influence is not significant. The partial electronic conductivity in the electrolyte induces a state-independent resistance $R_{\text{leak}}$ due to a leakage current in parallel. (c) Simulated $I$-$V$ characteristic of the extended memristor. The zoom shows the non-zero-crossing behaviour. Further considerations on the simulation are described in Supplementary Note 4.
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“Memristors” are reported to find applications in different fields:

- Non-volatile memory
- Analog circuits
- Logic circuits/computation
- Neuromorphic systems
  - (Image processing)
Are Memristors needed?

• Most interesting application:
  – combining analog signal processing with memory functionality!? (as e.g. neuromorphic systems)

• Important question:
  – what of these applications do follow from memristor theory?
  – or are they “just” demonstrated by “memristor-like” devices?

• Are “generalized” memristive system concepts as interesting as THE memristor
Some more “names”...
Memristors*: emulate synapse functionality

CMOS type

MEMRISTOR type

*Term coined by L.O. Chua, IEEE Transistor Circuit Theory 1971
Neuristors*: emulate axon signal transport

Figure 1 | Emulating an axon. Top: schematic diagram of a neuron. Bottom: spike generation and propagation along a chain of neuristors (N), mimicking the action potential propagating along an axon.

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A scalable neuristor built with Mott memristors
Matthew D. Pickett*, Gilberto Medeiros-Ribeiro and R. Stanley Williams

*Term coined by H.D. Crane, IRE 1960
Memistor ≠ Memristor!

Solid-state thin-film memistor for electronic neural networks

S. Thakoor, A. Moopenn, T. Daud, and A. P. Thakoor
Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California 91109

3132 J. Appl. Phys. 67 (6), 15 March 1990

FIG. 1. Schematic cross section of a three-terminal WO₃ memistor device.
Thank You !